Distributed by:

JAMECO® ELECTRONICS

www.Jameco.com ✦ 1-800-831-4242

The content and copyrights of the attached material are the property of its owner.

Jameco Part Number 163176

Document No TE-019-001
2nd Edition

ME DISPLAYS

USER'S GUIDE

MEG12864

128 x 64 dot matrix display
Chip On glass (COG)

Micro Electronics Corporation
3375 Scott Blvd. Suite 222 Santa Clara CA 95054
Tel: 408-988-1101 Fax: 408-988-7626
Email: micro@microelect.com
Http://www.microelect.com

CONTENTS

CHAPTER 1. INTRODUCTION TO MEG12864 CHIP ON GLASS

Features	1
Mechanical Specifications	1
Electrical Absolute Maximum Ratings	1
External Dimensions	2
Application Diagram	3
Interface Pin Connections	4
Temperature Characteristics	6
DC Electrical Characteristics	6

CHAPTER 2. DRIVER IC FUNCTION DESCRIPTION

Chip Select	7
Microprocessor Interface	7
Busy Flag	7
Display Timing Generation Circuit	8
Display Data RAM (DDRAM)	8
Data Transfer	10
Page Address Register	10
Column Address Counter	10
Display Start Line Register	10
LCD Driver	10
Reset Circuit	11

CHAPTER 3. INSTRUCTION DESCRIPTION

Detailed Instruction Description	12
AC Electrical Characteristics	14

CHAPTER 1.
INTRODUCTION TO MEG12864 CHIP ON GLASS

MEG12864 is a dot matrix graphic LCD module which is fabricated with Chip On Glass (COG) technology. It can display 128 x 64 dots size LCD panel using a 128 x 64 bit-mapped Display Data RAM (DDRAM). It interfaces with an 8-bit microprocessor.

FEATURES

- Display format : 128 x 64 dot matrix graphic
- STN yellow-green mode
- Easy Interface with 8 bit MPU
- Low power consumption
- Viewing Angle : 6 O'Clock
- Driving Method : 1/64 duty, 1/6.7 bias
- LCD Driver IC : KS0708
- COG Technology
  - Better Module thickness and size
  - Simpler Structure
  - Easy Process
  - High Reliability

MECHANICAL SPECIFICATIONS

Item	Dimension	Unit
Module size (W*H*T)	76.0 x 52.5 x 1.83	mm
Viewing Area (W*H)	720 x 40.0	mm
Dot Size (W*H)	0.48 x 0.48	mm
Dot Pitch (W*H)	0.52 x 0.52	mm

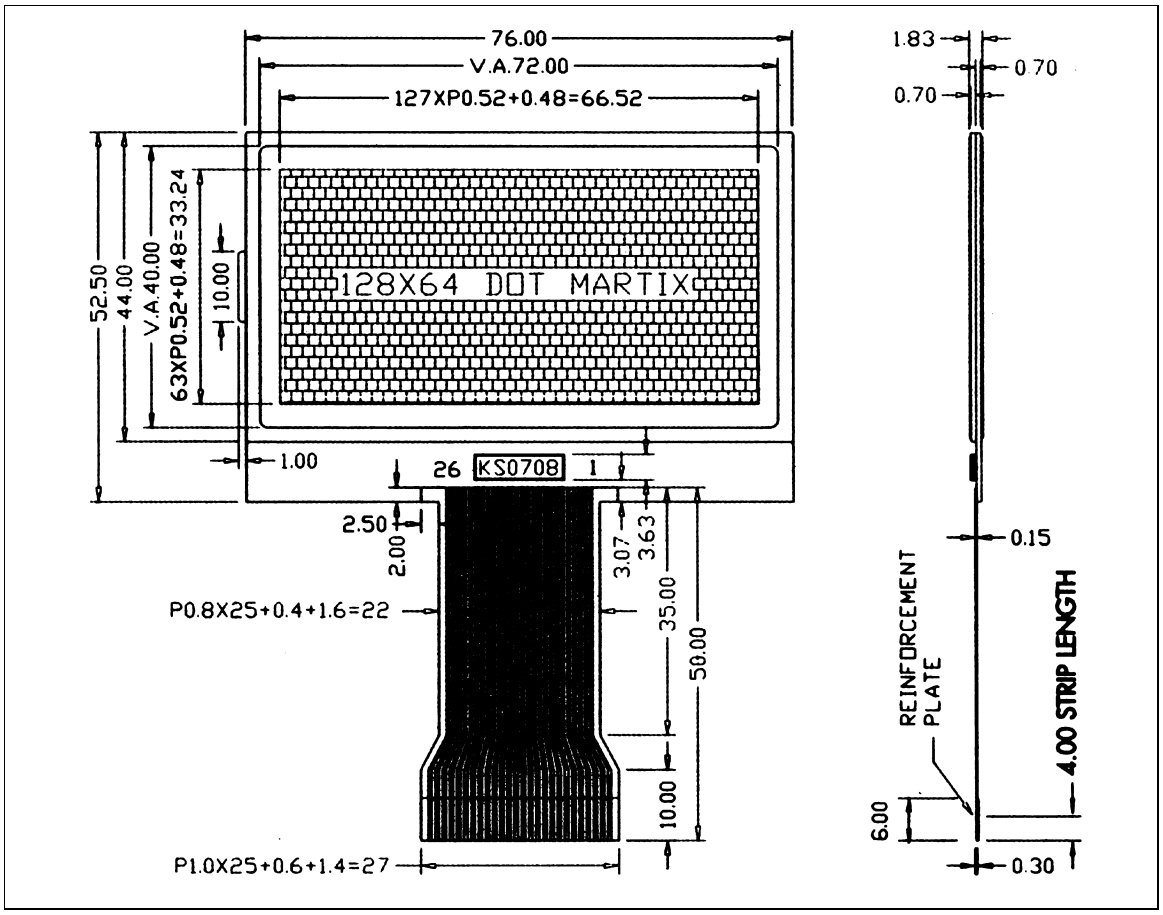
ELECTRICAL ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Operating Voltage	V_{DD}	-0.3 ~ +7.0	V	*1
Supply Voltage	V_{EE}	V_{DD} -19.0 ~ V_{DD} + 0.3	V	*4
Driver Supply Voltage	V_D	-0.3 ~ V_{DD} + 0.3	V	*1,*3
	V_{LCD}	V_{EE} - 0.3 ~ V_{DD} + 0.3	V	*2

Notes:
*1 : Based on V_{ss} - 0V
*2 : $V_{LCD} = V_{DD} - V_{EE}$
*3 : Applies to SHL. FS. PCLK2, CR, RESETB, ADC, CSLB, CS2B, E, RW, RS and DB0~DB7
*4 : Voltage Level

$V_{DD} \geq V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq V5 \geq V_{EE}$

FIGURE 1. EXTERNAL DIMENSIONS

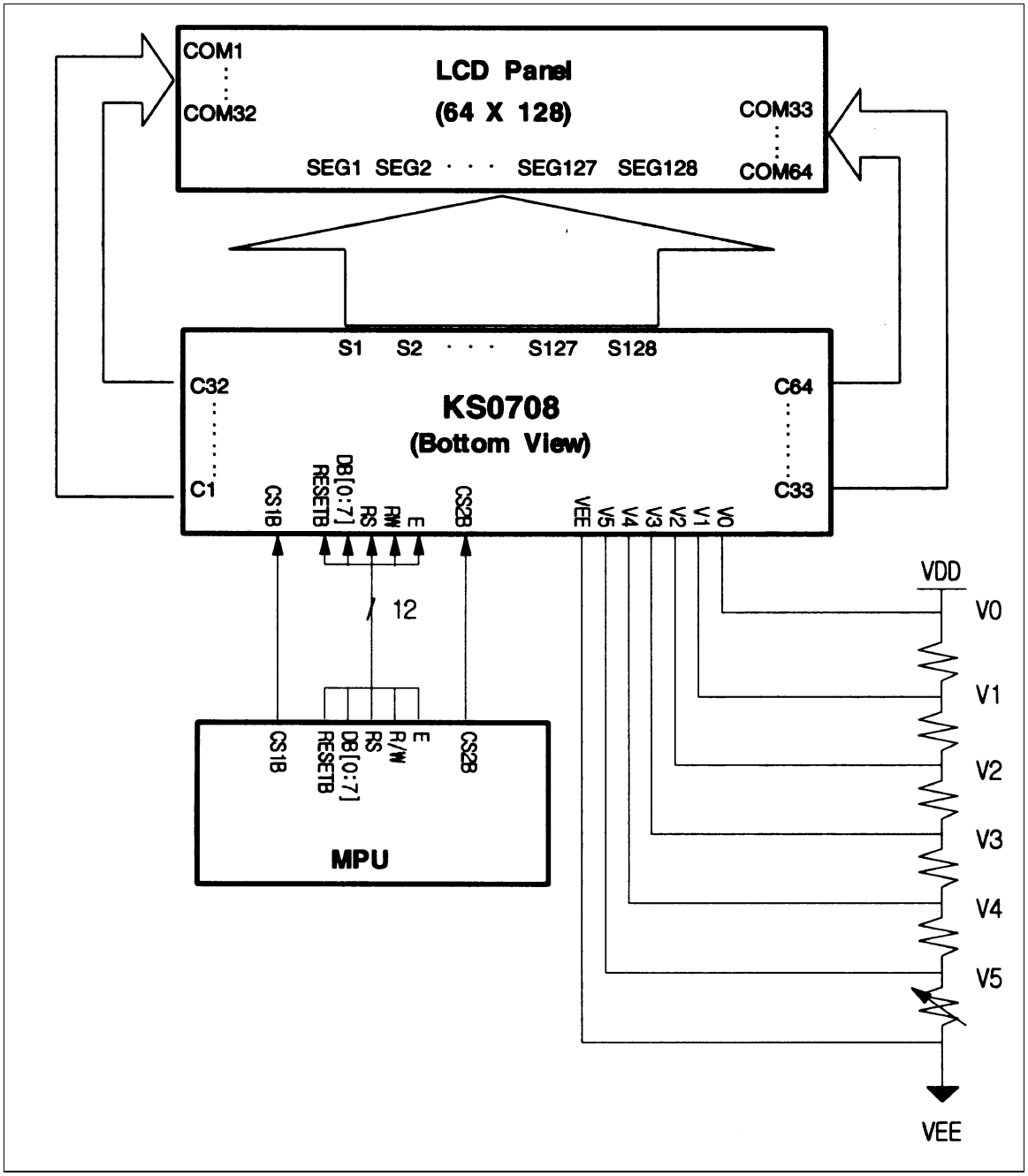


Dimensions in MM

PIN CONNECTIONS

Pin No	1	2	3	4	5	6	7	8	9	10
Signal	VEE	V5	V4	V3	V2	V1	VDD	VSS	PCLK2	CS2B
Pin No	11	12	13	14	15	16	17	18	19	20
Signal	C	CR	R	DB0	DB1	DB2	DB3	DB4	DB5	DB6
Pin No	21	22	23	24	25	26				
Signal	DB7	RS	RW	E	CS1B	RSTB				

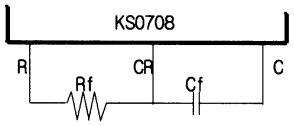
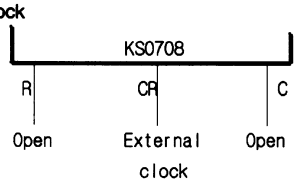
FIGURE 2. APPLICATION DIAGRAM



Note

FS = H, SHL = H, ADC = H

INTERFACE PIN CONNECTIONS

Pin No.	Symbol	I/O Type	Description
1	VEE	Supply	For LCD Driver Circuit
2 3 4 5 6	V5 V4 V3 V2 V1	Supply	LCD Driver Supply Voltages The voltages Must Satisfy the following relationship: $V_{DD} \geq V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq V5 \geq V_{EE}$
7	VDD	Supply	Power Supply
	V0	Supply	LCD Driver Supply Voltage
	FS	I	Frequency Selection When the frame frequency is 70HZ, the oscillation frequency should be as in the following table FS Oscillation Frequency H F_{osc} = 430kHz L F_{osc} = 215kHz
	SHL	I	Selection of data shift direction SHL Data Shift Direction H C1 → C2 → C3 …..… C62 → C63 → C64 L C64 → C63 → C62 ……. C3 → C2 → C1
	ADC	I	Address control signal of column address counter ADC Segment Output Direction H S1 → S2 … S63 → S64 →S65 → S66 …. S127 → S128 L S64 → S63 …. S2 → S1 → S128 S127 …. S66 → S65
8	VSS	Supply	Ground
9	PCLK2	I	Phase of Internal Shift Clock (CLK2) PCLK2 Phase of Internal Shift Clock (CLK2) H Data shift at the rising edge of CLK2 L Data shift at the falling edge of CLK2
10	CS2B	I	Second Chip (S65 - S128) select input Data input/output is enabled via E, RS, RW and DB[7:0] when CS2B = "low"
11 12 13	C CR R	O I O	RC Oscillator **i) Internal clock**  **ii) External clock** 

INTERFACE PIN CONNECTIONS (CONT)

Pin No.	Symbol	I/O Type	Description
14 15 16 17 18 19 20 21	DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7	I/O	Data Bus (0-7) Bi-Directional Data Bus
22	RS	I	Register Selection RS Description H The data in DB [7:0] is display data L The data in DB [7:0] is control data
23	RW	I	Read or Write RW Description H Data appears at DB [7:0] when E=High L Display data DB [7:0] can be written at falling edge of E
24	E		Enable Signal E Description H Read data in DB [7:0] appears while E = “High” L Display data DB [7:0] is latched at falling edge of E
25	CS1B	I	First Chip (S1 ~ S64) Select Input Data input/output is enabled via E, RS, RW, and DB [7:0] when CS1B = “Low”
26	RESETB	I	Reset Input Chip is initialized when RESETB is “Low”

TEMPERATURE CHARACTERISTICS

Parameter	Symbol	Rating	Unit
Operating Temperature	T_{opr}	-20 ~ +70	°C
Storage Temperature	T_{stg}	-30 ~ +80	°C

DC ELECTRICAL CHARACTERISTICS

(VDD = 4.5 to 5.5V, Ta = -20 to +70 °C)

Item	**Symbol**	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**	**Note**
Operating Voltage	V_{DD}	--	4.5	-	5.5	V	
Input High Voltage	V_{IH1}	--	0.7 V_{DD}	-	V_{DD}	V	*1
	V_{IH2}	--	2.0	-	V_{DD}		*2
Input Low Voltage	V_{IL1}	--	0	-	0.3 V_{DD}	V	*1
	V_{IL2}	--	0	-	0.8		*2
Output High Voltage	V_{OH}	I_{OH} = -200uA	2.4	-	-	V	*3
Output Low Voltage	V_{OL}	I_{OL} = 1.6mA	-	-	0.4	V	*3
Input Leakage Current	I_{LKG}	$V_{IN} = V_{SS}$ - V_{DD}	-1.0	-	+1.0	uA	*4
Tri-State Leakage Current	I_{LKG}	$V_{IN} = V_{SS}$ - V_{DD}	-5.0	-	+5.0	uA	*5
Driver Input Leakage Current	I_{DLKG}	$V_{IN} = V_{EE}$ -V_{DD}	-10.0	-	+10.0	uA	*6
Operating Current	I_{DD1}	during display	-	-	0.8	mA	*7
	I_{DD2}	during access	-	-	1.0	mA	*8
On Resistance -- COM	R_{ONC}	VDD - VEE = 17V ± ILOAD	-	-	1.5	kΩ	*9
On Resistance –SEG	R_{ONS}	I_{OAD}= 0.1mA	-	-	7.5	kΩ	*10
Oscillation Frequency	f_{OSC}	Ta = 25°C, V_{DD} = 5V Rf = 47kΩ ± 2% Cf = 20pF ± 5%	315	450	585	KHz	

NOTES
*1 : FS, CR, ADC, SHL, PCLK2, RESETB
*2 : CS1B, CS2B, E, RW, RS, DB0~DB7
*3 : DB0~DB7
*4 : Except DB0~DB7
*5 : DB0-DB7 at high impedance
*6 : V0, V1, V2, V3, V4, V5
*7 : C=20pF, R=47kΩ, fosc=450kHz, DB0~DB7=VDD, output - No load
*8 : External clock = 500kHz, RAM access cycles – 1MHz
*9 : V0 = 5V, V1 = 3.2V, V2 = 1.4V, V3 = -8.4V, V4 = -10.2V, V5 = -12V, C1~C64
*10 : V0 = 5V, V1 = 3.2V, V2 = 1.4V, V3 = -8.4V, V4 = -10.2V, V5 = -12V, S1 ~ S128

CHAPTER 2.
DRIVER IC FUNCTION DESCRIPTION

KS0708 DRIVER IC
64COM / 128SEG GRAPHIC DRIVER FOR DOT MATRIX LCD

CHIP SELECT

The KS0708 has two Chip Select pins, CS1B and CS2B. It can interface with a microprocessor when either CS1B or CS2B is "Low". When both of these pins are set to "High", DB0 to BD7 are at high impedance and RS, RW, and E inputs are disabled.

CS1B pin controls the display status of S1 to S64, and CS2B does that of S65 to S128. When CS1B and CS2B are "Low" at the same time. It is impossible to execute read operation. Therefore, one of CS1B or CS2B should be set to "Low" ((CS1B – "L" & CS2B – "H")) in read operation. The RESETB signal is entered independent of the status of Chip Select.

Table 1. Relationship between Chip Select Pins and Read/Write Operation

CS1B	CS2B	Read Operation		Write Operation	
		CS1	CS2	CS1	CS2
H	H	X	X	X	X
L	H	O	X	O	X
H	L	X	O	X	O
L	L	--	--	O	O

-- : Not Recommended, O : Operation, X : No Operation

MICROPROCESSOR INTERFACE

KS0708 transfers 8-bit parallel data bi-directionally between the controlling microprocessor and the KS0708 through the 8-bit I/O buffer (DB0 to DB7)

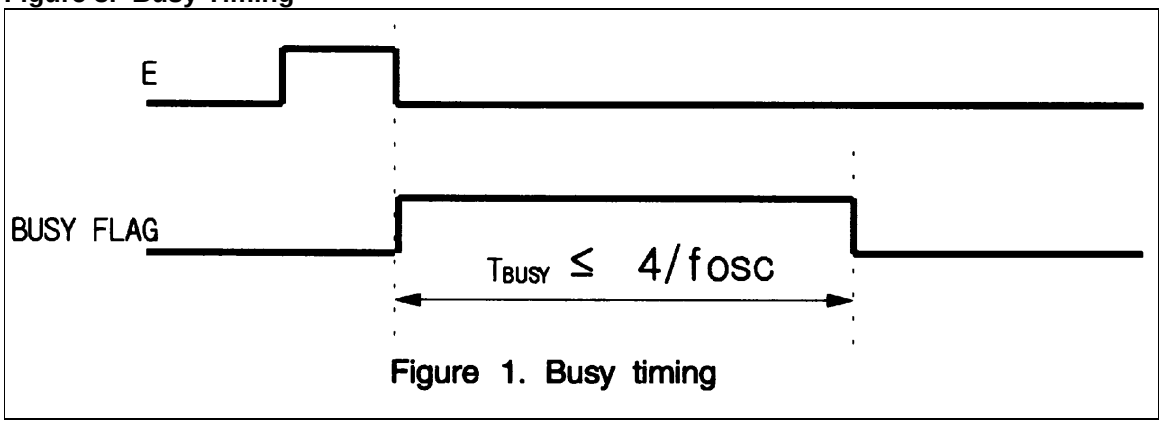
RS, RW and E identify the type of parallel data transfer to be made as shown below in Table 2.

Table 2. Microprocessor Interface

RS	RW	Description
H	H	Read Display Data
H	L	Write Display Data
L	H	Status Read
L	L	Write to Internal Register (instruction)

BUSY FLAG
Busy Flag indicates whether KS0708 is operating or not. When it is "High", KS0708 is in internal operation. When it is "Low", KS0708 can accept the data or instruction. DB7 indicates KS0708's Busy Flag.

Figure 3. Busy Timing



DISPLAY TIMING GENERATION CIRCUIT

- Generates the signal to the display start line counter and the display data latch circuit
- The display clock (CLK2) generates a clock to the line counter. The display start line address of the display RAM is synchronized with the display clock. 128-bit display data is latched by the display data latch circuit in synchronization with the display clock and output to the segment LCD drive output pin.
- Generates the LCD AC signal (M).

DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD panel. It is a 128 - column by 64 - row addressable array as shown in Table 3.

The 64 - rows are divide into 8 - pages of 8 - lines. Data is read from or written to the 8 - lines of each page directly through DB0 to DB7.

The microprocessor reads data from or writes data to DDRAM through the I/O buffer. Since the LCD controller operates independently, data can be written to the DDRAM at the same time as the data is being displayed.

Figure 4. RAM to LCD Panel Data Transfer.

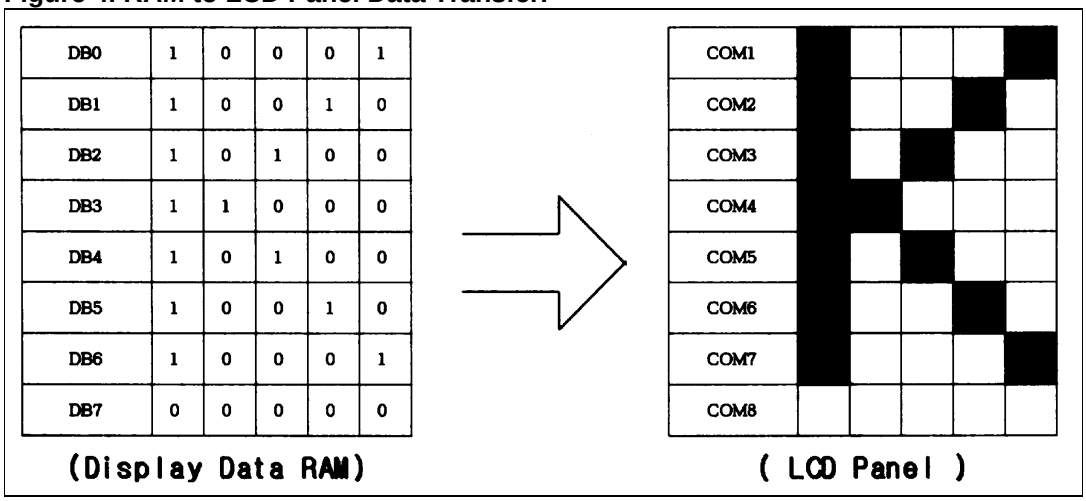


Table 3. Display Data RAM

Page address	Line address	SEGMENT OUTPUT(S1 ~ S64)									DATA BUS	SEGMENT OUTPUT(S65 ~ S128)									Line address	Page address
		S1	S2	S3	S4	.....	S61	S62	S63	S64		S65	S66	S67	S68	.....	S125	S126	S127	S128		
000	00 01 02 03 04 05 06 07					.....					DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7					.....					00 01 02 03 04 05 06 07	000
001	08 09 10 11 12 13 14 15					.....					DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7					.....					08 09 10 11 12 13 14 15	001
010	16 17 18 19 20 21 22 23					.....					DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7					.....					16 17 18 19 20 21 22 23	010
011	24 25 26 27 28 29 30 31					.....					DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7					.....					24 25 26 27 28 29 30 31	011
100	32 33 34 35 36 37 38 39					.....					DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7					.....					32 33 34 35 36 37 38 39	100
101	40 41 42 43 44 45 46 47					.....					DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7					.....					40 41 42 43 44 45 46 47	101
110	48 49 50 51 52 53 54 55					.....					DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7					.....					48 49 50 51 52 53 54 55	110
111	56 57 58 59 60 61 62 63					.....					DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7					.....					56 57 58 59 60 61 62 63	111
ADC	1	0	1	2	4	.....	60	61	62	63		0	1	2	4	.....	60	61	62	63	1	ADC
	0	63	62	61	60	.....	3	2	1	0		63	62	61	60	.....	3	2	1	0	0	
		Column address										Column address										
		Chip Select (CS1B)										Chip Select (CS2B)										

DATA TRANSFER

To match the timing of the Display Data RAM and registering to that of the controlling microprocessor, KS0708 uses an internal data bus and bus buffer. When the microprocessor read the contents of the display Data RAM, the data for the initial read cycle is first stored in the bus buffer (dummy read cycle). On the next read cycle, the data is read from the bus buffer onto the microprocessor bus. At the same time, the next block of data is transferred from RAM to the bus buffer. Otherwise, when the microprocessor write data to display data RAM, the data is written to RAM after the falling edge of the E signal. Therefore, it is necessary to check Busy Flag to write or read the next data.

PAGE ADDRESS REGISTER

The 3-bit Page Address register provides the page address to the Display Data RAM (refer to Table 3). The microprocessor issues Set Page Address Instructions to change the page and to access another page.

COLUMN ADDRESS COUNTER

The column address counter is a 6-bit pre-settable counter that provides the column address to display data RAM (refer to Table 3). It is automatically incremented by 1 after execution of each Read/Write data instruction. The column address counter loops the values 0 to 63, and it is independent of page address register. The ADC pin is issued to change the relationship between RAM column address and display segment output.

DISPLAY START LINE REGISTER

The display start line register stores the line address of display data RAM that corresponds to the first (normally the top) line (COM1) of liquid crystal display panel. See Table 1. When displaying contents in display data RAM on the LCD panel, 6-bit data (DB[5:0]) of the set display start line is latched in the display start line register. Latched data are transferred to the line address counter just before COM1 is active “High”, pre-setting the line address counter. The line counter then incremented on the display latch clock signal once for every display line. It is used for vertical scrolling of the liquid crystal display.

LCD DRIVER

LCD Driver circuit has 192 outputs of 128 segment outputs, 64 common outputs for LCD driving. Each common output has a shift register. LCD driving output voltage is determined by the combination of display data and internal AC signal.

Table 4. Relationship Between Data for Each Input Signal and the LCD Drive Output

Display Data	Common Output	Segment Output
0	V1	V2
	V4	V3
1	V5	V0
	V0	V5
Display off		V2 or V3

RESET CIRCUIT

Reset function can initialize the system by setting RESETB terminal “Low”, When RESETB becomes “Low”, following procedure occurs.

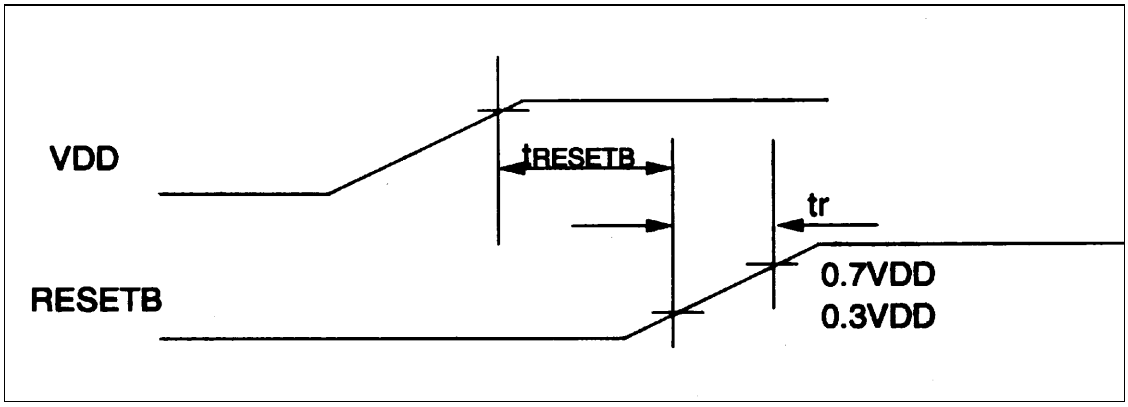
- Display start line : 0 (first)
- Display ON/OFF : Off

While RESETB is “Low”, no instruction except Status Read can be accepted. When executing the Status Read Instruction, the reset status can be read at the DB4 pin. The conditions of power supply at initial power up are shown in Table 5.

Table 5. Power Supply Initial Conditions

Item	Symbol	Min	Typ	Max	Unit
Reset Time	t_{RESETB}	1.0	--	--	u S
Rise Time	t_R	--	--	200	u S

Figure 6. Reset Timing



CHAPTER 3.
INSTRUCTION DESCRIPTION

Table 6. Instruction Descriptions

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Functions
Read Display Date	1	1	Read Data								Reads data (DB[7:0]) from DDRAM to the data bus.
Write Display Date	1	0	Write Data								Writes data (DB[7:0]) into the DDRAM. After writing instruction column address is incremented by 1 automatically
Status Read	0	1	Busy	0	ON / OFF	Re-set	0	0	0	0	Reads the internal status BUSY -0: Read -1: In operation ON/OFF -0: Display ON -1: Display OFF RESET -0: Normal -1: Reset
Set Column Address	0	0	0	1	Column Address (0-63)						Sets the column address at the column address counter
Set Display Start Line	0	0	1	1	Display Start Line (0-63)						Indicates the Display Data RAM displayed at the top of the screen
Set Page Address	0	0	1	0	1	1	1	Page (0-7)			Sets the page address at the page address register
Display On/Off	0	0	0	0	1	1	1	1	1	0/1	Controls the display ON or OFF. The internal status and the DDRAM data is not affected. 0: OFF; 1:ON

DETAILED INSTRUCTION DESCRIPTIONS

READ DISPLAY DATA

Read 8-bit data in the Display Data RAM area specified by column address and page address. As the column address is automatically incremented by 1 after each read operation, the microprocessor can continue to read data of multiple words.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read Data							

WRITE DISPLAY DATA

Write 8-bit data in display data RAM. As the column address is incremented by 1 automatically after each write operation, the microprocessor can continue to write data of multiple words.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Write Data							

STATUS READ
Indicates the internal status conditions of the device to the microprocessor.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Busy	0	ON/OFF	RESET	0	0	0	0

Flag	Description
BUSY	The device is busy due to internal operation or reset. All instructions are rejected until BUSY goes “Low”.
ON/OFF	Indicates whether the display is on or off. When low, the display is on. When high, the display is off. This is opposite Display ON/OFF instruction.
RESET	Indicates the initialization is in progress by RESETB signal. When low, the chip is active. When high, the chip is being reset.

SET PAGE ADDRESS
Sets the page address of display RAM from the microprocessor into the page address register. Along with the column address register. Page address register assigns the address of the display RAM to be written to or lead from display data. Changing the address doesn’t affect the display status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	1	0	1	1	1	X2	X1	X0

X2	X1	X0	Page
0	0	0	0
0	0	1	1
:	:	:	:
1	1	1	7

SET COLUMN ADDRESS
Sets the Column address of display RAM from the microprocessor into the column address register. When the microprocessor reads or writes display data to our from display RAM, the addresses are automatically incremented.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	Y5	Y4	Y3	Y2	Y1	Y0

Y5	Y4	Y3	Y2	Y1	Y0	Column Address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

SET DISPLAY START LINE
Sets the line address of display RAM to determine the display start line. The display data on the specified line of the display RAM is displayed at the top row COM1 of the LCD panel. It is followed by higher number of lines in ascending order, corresponding to the determined duty cycle. When this instruction changes the display start line address, the LCD panel can scrolled.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	Z5	Z4	Z3	Z2	Z1	Z0

Z5	**Z4**	**Z3**	**Z2**	**Z1**	**Z0**	**Line Address**
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

DISPLAY ON/OFF
Turns the display On or Off

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	1	D0

D0 = 1: Display On
D0 = 0: Display Off

AC ELECTRICAL CHARACTERISTICS

Mode	**Item**	**Symbol**	**Min**	**Typ.**	**Max.**	**Unit**
Write Mode	E cycle time	T_{cyc}	1000	--	--	ns
(Refer to	E rise/fall time	T_r , T_f	--	--	25	
Figure 7)	E pulse width high	t_{pWH}	450	--	--	
	RW and RS setup time	t_{AS}	140	--	--	
	RW and RS hold time	t_{AH}	10	--	--	
	Data setup time	t_{DS}	200	--	--	
	Data hold time	t_{OH}	10	--	--	
Read Mode	E cycle time	T_{cyc}	1000	--	--	ns
(Refer to	E rise/fall time	T_r, T_f	--	--	25	
Figure 8)	E pulse width high	T_{pWH}	450	--	--	
	RW and RS setup time	T_{AS}	140	--	--	
	RW and RS hold time	T_{AH}	10	--	--	
	Data output time	T_O	--	--	320	
	Data hold time	T_{OH}	20	--	--	

Figure 7. Write Mode Timing Diagram

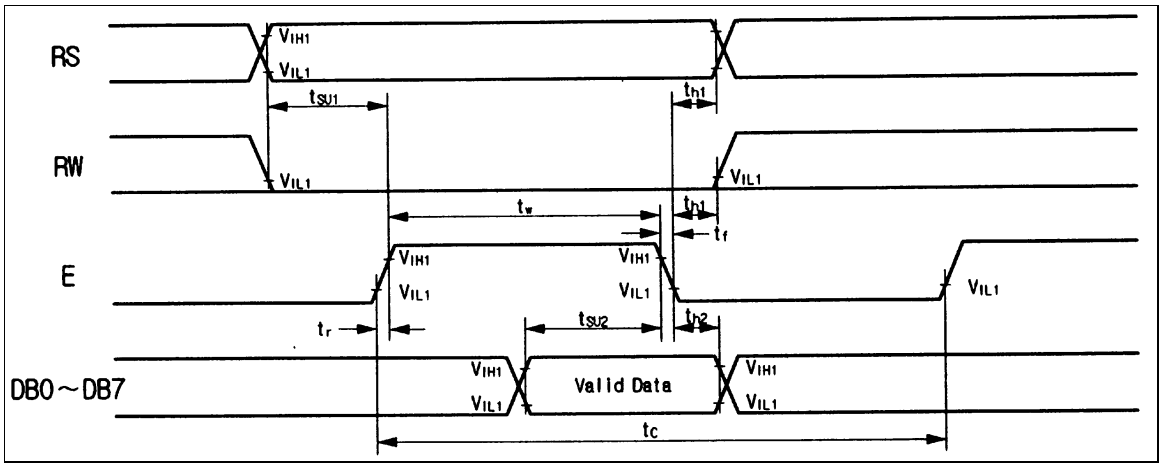


Figure 8. Read Mode Timing Diagram